

Fabrication and Characterization of Au/Si Heterojunction Solar Cell

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ARTICLE INFO

Volume 3
Number 5/2014
Issue 9
DOI Prefix: [10.15590/ajase/](https://doi.org/10.15590/ajase/)

Received: Sep 21, 2014
Accepted: Dec 03, 2014
Revised: Dec 05, 2014
Published: Jan 04, 2015
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ABSTRACT

The n-type Au thin films of 500nm thickness was evaporated by thermal evaporation method on p-type silicon wafer of [111] direction to formed Au/Si heterojunction solar cell.

The AC conductivity, C-V and I-V characteristics of fabricated c-Au/Si diffusion heterojunction-(HJ) solar cell, has been studied. The first methods demonstrated that the AC conductivity due to with diffusion-tunneling mechanism, while the second show that, the heterojunction profile is abrupt, the heterojunction parameters have been played out, such as the depletion width, built-in voltage, and concentration.

And finally the third one show that the c-Au/Si HJ has rectification properties, and the solar cell yielded an open circuit voltage of (V_{ic}) 0.4V, short circuit current (I_{sc}) of 2.01mA, fill factor (F.F) of 0.085 and $\eta\% = 7.19$.

Keywords: Au thin films, C-V and I-V characteristics, Au/ Si heterojunction, solar cell parameters

Source of Support: Nil, Conflict of Interest: Declared.

How to Cite: Khudayer IH. 2014. **Fabrication and Characterization of Au/Si Heterojunction Solar Cell** *Asian Journal of Applied Science and Engineering*, 3, 34-44.

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INTRODUCTION

Metal-semiconductor interfaces have been studied extensively owing to their variety of interesting properties that are both scientifically and technologically significant.

The Au/Si interface has been of interest due to the possible application as a metal-Si contact in integrated circuit devices. As Au atoms diffuse very fast and serve as deep-trap centers in Si, Au/Si contacts have been found unsuitable for this purpose. But the interface is of interest for fundamental reasons. Though gold is usually considered as a

nonreactive stable noble metal, it has been described to be very reactive on Si surfaces, even at room temperature (Sundaravel etel, 1999; Hong etel, 2005; and Bokhonov & Korchagin, 2000).

Beginning in the early 1970s, the gold-silicon interface has been extensively investigated using various surface techniques to understand its crystallographic, chemical, and electronic properties. Despite the Au/Si contact being unsuitable for applications in integrated circuit devices due to the rapid dispersion of Au atoms and their bass-trap center formation in Si, the study of thin gold films on Si still raises interesting questions. Regions of interest include the supposed Au-Si reaction at room temperature (RT) and the critical gold coverage necessary to induce it, the diffusion of sin through Au layers even for thick deposits, and related properties such as the source and construction of electronic states at the interface. A non-exhaustive list of the techniques used, individually or combined, includes low-energy electron diffraction (LEED), Auger electron spectroscopy (AES), MeV ion backscattering, electron-energy-loss spectroscopy (EELS), x-ray photoelectron spectroscopy (XPS), ultraviolet photoelectron spectroscopy (UPS), photoemission yield spectroscopy, soft x-ray photoelectron spectroscopy, scanning tunneling microscopy (STM), x-ray standing wave, and transmission electron microscopy (TEM) (Hazra, 2007; Landry etel, 1997).

EXPERIMENTAL PARTS

Thin films of high purity Au 99.99% have been deposited on silicon by thermal evaporation technique at room temperature, in a high vacuum system of (3×10^{-6}) Torr using the Edward coating unit model (E 306) from molybdenum boat, the distance between the boat and the substrate was about 15 cm. Film thickness was about (500 ± 50) nm at R.T (300 K) with a deposition rate (1.5 nm/Sec) to form a heterojunction solar cell. Ohmic contacts are made on both Au thin films and Si substrate by depositing of Al films through certain mask.

X-ray Diffraction (XRD): was used to the position and intensity of diffracted intensity spectra versus Bragg's angle, gives information on the crystal structure such as phase crystalline, polycrystalline, amorphous, grain size, and lattice parameter.

The inter planer distance d (kl) for different planes was measured by Bragg's law (Blackmore, 1974):

$$2d\sin\theta = n \quad (1)$$

The structures of the alloy and deposited films have been examined by XRD methods using the Siemens x-ray diffractometer system.

The capacitance of the heterojunction is measured as a function of the bias voltage in reverse bias in the range (from 0 to -2) Volt with different values of frequency in the range 10^5 - 3×10^6 Hz uses model 4274A and 4275A multi-frequency LRC meter.

In addition, a convenient formalism to investigate the frequency behavior of conductivity is based on the power law relation proposed by Jonscher (Ertuğrul, 2012):

$$(\omega) = \sigma_{dc} + \sigma_{ac} = \sigma_{dc} + A\omega^s \quad (2)$$

Where, (ω) is the total conductivity. The first term is the temperature-dependent (frequency-independent) DC conductivity and relates to the drift mobility of the electric charge carriers. The second term represents the frequency and temperature dependent ac conductivity (σ_{ac}) and is attributed to the dielectric relaxation caused by the localized

electric charge carriers. Is a temperature-dependent constant and s is the power law frequency exponent which generally varies between 0 and one (Ertuğrul, 2012).

Capacitance voltage measurements can be manipulated to yield a number of parameters such as: type of the junction (abrupt or graded), built-in voltage (V_D) was obtained from the intercept at $(1/C^2) = 0$ by extrapolating the curve to the voltage axis. Carrier concentration and the width of the junction (depletion layer) can be deduced from the following equation (Grove, 1976):

$$W = \frac{\epsilon_s}{\epsilon_o} \quad (3)$$

Where, C_o is the capacitance at zero biasing voltage, and

$$\epsilon_s = \frac{\epsilon_n \epsilon_p}{\epsilon_n + \epsilon_p} \quad (4)$$

Where ϵ_s is the semiconductor permittivity for the two semiconductor materials. The concentration of the carrier was calculated from the relation (Milnes & Feucht, 1972):

$$\frac{1}{C^2} = \left[\frac{2(\epsilon_1 N_{A1} + \epsilon_2 N_{D2})}{q N_{D2} N_{A1} \epsilon_1 \epsilon_2} (V_D - V_a) \right] \quad (5)$$

Where $[2(\epsilon_1 N_{A1} + \epsilon_2 N_{D2}) / q N_{D2} N_{A1} \epsilon_1 \epsilon_2]$ represent the slope, N_{A1} and N_{D2} are the acceptor and donor concentrations, and ϵ_1 , ϵ_2 are the dielectric constant of p-type and n-type semiconductor respectively. V_D is the built-in potential, V_a is the applied voltage.

I-V characteristics have been practiced through the dark current-potential measurement for Au/Si, which, carried out using applying a voltage to the sample from a stabilized d.c fine power supply. The current going through the device was evaluated utilizing a digital electrometer (Keithley 616). The bias voltage was varied (0-1.5) Volt in the case of forward and reverse bias.

From the plot of the dark forward current as a function of bias voltage, the ideality factor was determined from the relation (Sharma & Purohil, 1974):

$$\beta = \frac{q}{k_B T} \frac{V}{\ln(I_f / I_{s1})} \quad (6)$$

The tunneling constant A was deduced from the equation:

$$A = \frac{d \ln(I_f / I_{s2})}{dV} \quad (7)$$

The ideality factor (β) and the saturation current (I_s) can be used to determine the theoretical value of the zero-bias resistance (R_o) of the photodiode using a simple formula (Wenus etel, 2003):

$$R_o = \frac{\beta K T}{q I_s} \quad (8)$$

While the rectification factor (RF) was calculated according to the following equation (Sze, 1981):

$$R.F = \frac{I_F}{I_R} \quad \text{for } V \geq 3kT/q \quad (9)$$

In the light condition, the optoelectronic measurements of heterojunction were made, the samples were exposed to halogen lamp at an intensity equal to $(1000) \text{ W/m}^2$.

In the absence of recombination or generation of carriers in the depletion region, J_R is voltage independent and is equal to the short-circuit photocurrent density (J_{SC}) (Dereniak & Crowe, 1992).

The open-circuit voltage V_{ic} across the heterojunction (i.e. for $J=0$) can process in terms of J_R and J_S as follows:

$$V_{ic} = \frac{k_B T}{e \ln(1 + J_R/J_S)} \quad (10)$$

The fill factor is defined as:

$$F.F = \frac{V_m I_m}{V_{oc} I_{sc}} \quad (11)$$

Where: $V_m I_m$ present the maximum power P_m .

$$\eta = \frac{P_m}{P_{in}} \times 100\% \quad (12)$$

RESULTS AND DISCUSSION

Fig. (1) shows that there was a diffusion process between P-Si substrate and Au n-type layers, which presented in the reflected diffraction angles at ($2\theta=38.42^\circ$ and 44.66°), revealed that there was present of Au-Si bonding in the formed Au/Si heterojunction, which illustrated that there was Au inclusion with the silicon wafer.

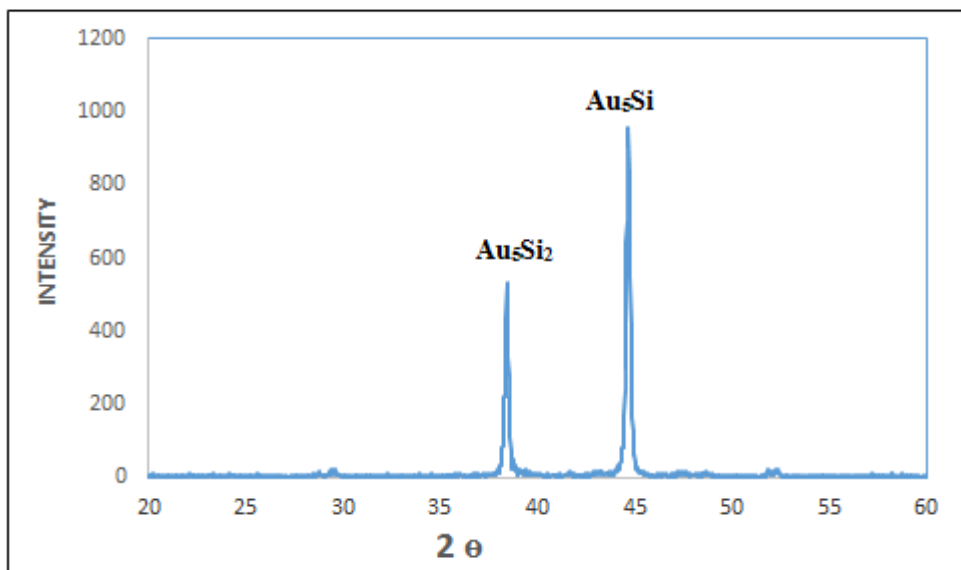


Fig. (1) Present XRD pattern of Au/Si heterojunction.

Two types of capacitances are associated with a diode junction. One capacitance, known as diffusion capacitance, is relative to the diode current, in a forward-biased diode, minority carriers are injected into opposite sides of the conjunction. Note that the diffusion capacitance does not depend on the junction area, but it only depends on the diode current.

Second capacitance, known as the depletion capacitance, reversed-biased diode looks like a capacitor with two "plates" formed of p-type and n-type regions, is a weak function of the applied voltage, and the dielectric layer (depletion region) between them (Irwin, 2011).

The analysis of the C-V measurements of the Au/Si only at one or narrow frequency and bias voltage range cannot give us detailed information about conduction mechanisms, the barrier formation. In contrary to, in a wide frequency and the bias voltage region, the C-V measurements of these devices can allow us to understand different aspects of conduction mechanisms. Thus, the C-V-f characteristics of Au/Si heterostructure have been investigated in a broad frequency range of 105Hz-3x106Hz.

Fig. 2, shows the capacitance variation as a function of frequency in the voltage of the range 0.5 to 2 V, with the step of 0.5 V as a parameter. The measured capacitances decrease with increasing frequency.

As can be seen in Fig.2, the measured capacitance and decrease with increasing frequency in the frequency range of 10⁴ Hz to 3x10⁶Hz. Such behaviour of the C attributed to a particular distribution of interface states. At low frequencies, the localized states can easily follow the AC signal and yield an excess capacitance, which depends on frequency and time constant of interface states. However, in sufficiently high frequency limit (f ≥1000 Hz), the localized can hardly follow the AC signal and the contribution of interface state capacitance to the total capacitance may be neglected (Arsel, 2012; TAŞÇIOĞLU etel, 2010).

At low frequencies, the charges on neutral impurity defects are more readily redistributed, such that defects closer to the positive side of the applied field become negatively charged while the defects closer to the negative side of the field become positively charged. As the frequency is increased, the capacitance decreases to the same limit, as the charges on the defects no longer have time to rearrange in response to the applied voltage (Ertuğrul, 2012; Ataseven & Tataroğlu, 2013).

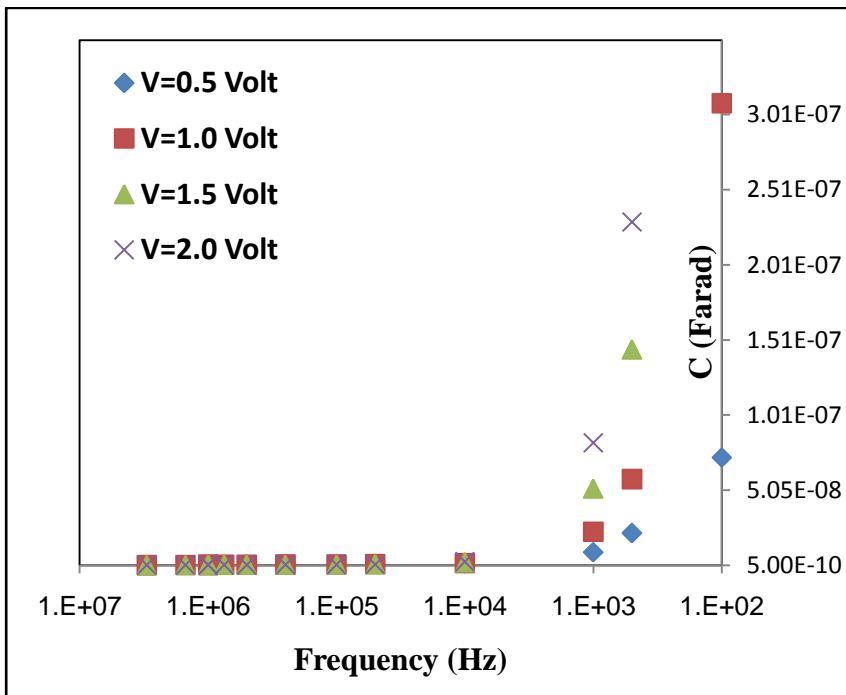


Fig.2 The capacitance-frequency characteristics of Au/Si heterostructure for various biases.

Fig.3 shows the $\ln\sigma_{ac}$ vs. $\ln f$ to illustrate the frequency dependence of AC - conductivity for heterojunction structure at various values of voltage. The σ_{ac} increases with the increasing frequency. The value of s for each voltage is determined from the slopes of $\ln\sigma_{ac}$ vs. $\ln f$ (Fig. 3).

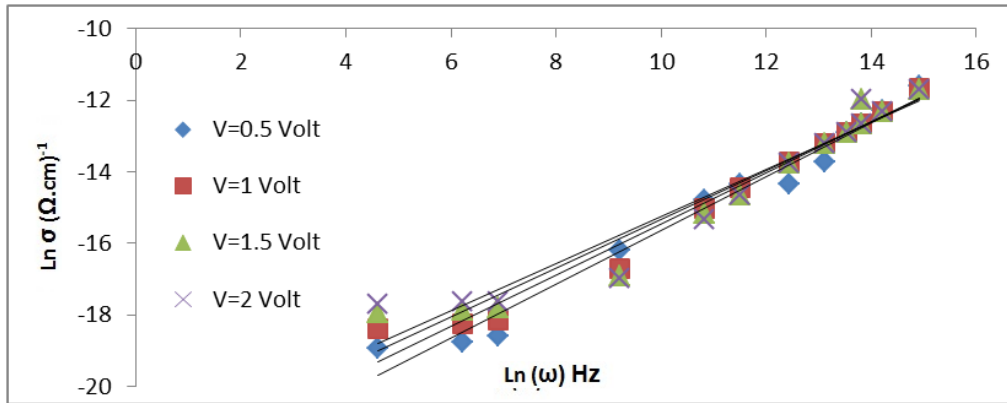


Fig.3 frequency dependences of the Ac conductivity of the Au/Si heterostructure at different voltages

Fig. 4 shows the voltage dependence of frequency exponent s for the heterojunction structure. It is observe that the s decreases with increasing voltage. The s values were found to change from 0.75 to 0.65 within the experimental voltage range the voltage - dependent parameter s represents the extent of interactions among charge carriers and defect states, these values of s indicated that the mechanism transport was due to tunneling between localized states near Fermi level according to QMT model.

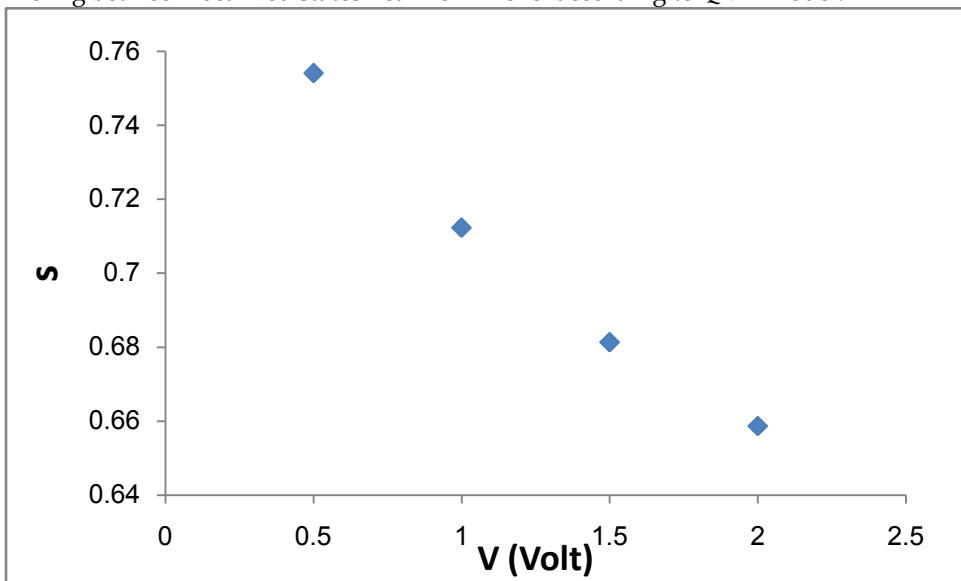


Fig.4 voltage dependencies of the s of the Au/Si heterostructure

The capacitance - voltage characteristics of Au/Si heterojunction with different values of frequency (10^5 - 3×10^6) Hz are shown in fig. 5. This measurement was considered in order to make an estimate about the impurity distribution in the vicinity of the articulation. The capacitance is expected to decrease with increasing reverse bias, due to an increase in the depletion region width, and it is clear from this figure the reduction was non-linear. Additionally, it can observe that the capacitance at zero bias voltage (C_o) was the decrease from 1.83×10^{-9} to 7.07×10^{-10} nF as the frequency increases. Fig.6 reveals the reciprocal of square capacitance versus reverse bias voltage. The linearity characteristic of this plot confirms that the junction is abrupt type. From the intercept on the x-axis and the slope of the best fit straight line, the built in voltage and an impurity concentration of donors can be obtained respectively. Table (1) illustrates all the parameters that are calculated from this measurement.

The value of built in voltage (V_D) increases from 0.50 to 0.85 V with increases the frequency values.

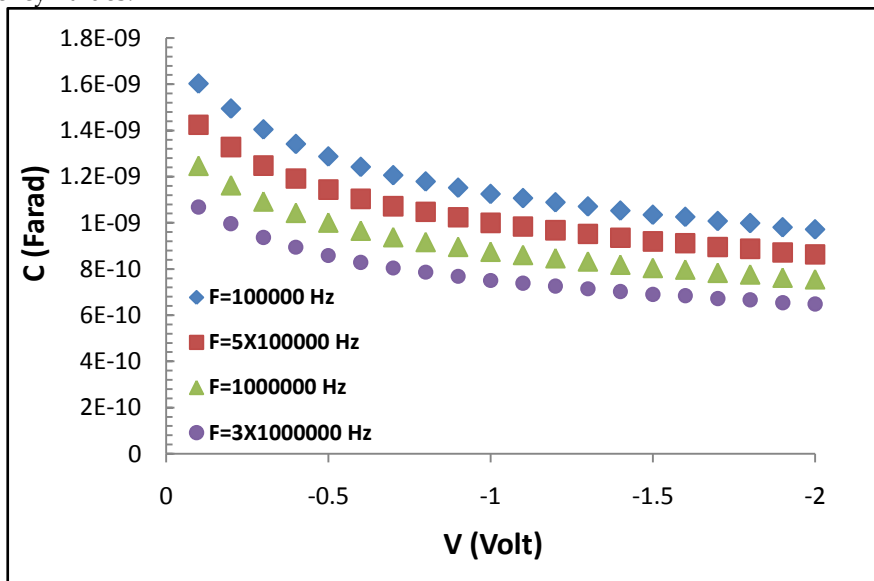


Fig.5 The relation between capacitance and reverse applied voltage of Au/Si heterostructure.

Table 1: Present the parameter that deduced from C-V measurements.

Frequency (Hz)	$N_D \times 10^{14} \text{ (cm}^{-3}\text{)}$	$W \text{ (}\mu\text{m)}$	$C_o \text{ (nF)}$	$V_D \text{ (Volt)}$
10^5	3.53	0.342	$1.83E-09$	0.50
5×10^5	2.65	0.559	$1.52E-09$	0.61
10^6	1.77	0.625	$1.01E-09$	0.74
3×10^6	1.32	0.884	$7.07E-10$	0.85

More thorough analysis of the current-voltage characteristics is necessary to specify the current mechanisms. A measured current - voltage plot which represent forward and reverse bias voltage under dark and light conditions of Au/Si heterojunction is shown in fig. 7.

In the case of the dark condition, the ratio between forward and reverse current at certain applied voltage represents the rectification coefficient (B) has been found out and it was found equal to 10, which indicated that this heterojunction has good rectification properties, which is in agreement with Fu Xiao-Nana et.al (Nana etel, 2012).

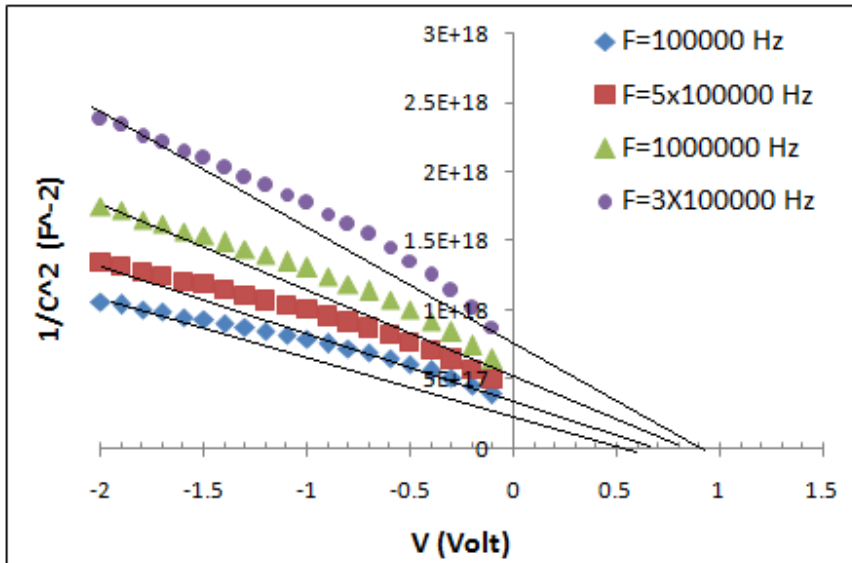


Fig.6 The variation of $1/C^2$ as a function of reverse bias voltage for Au/Si heterostructure at different frequencies

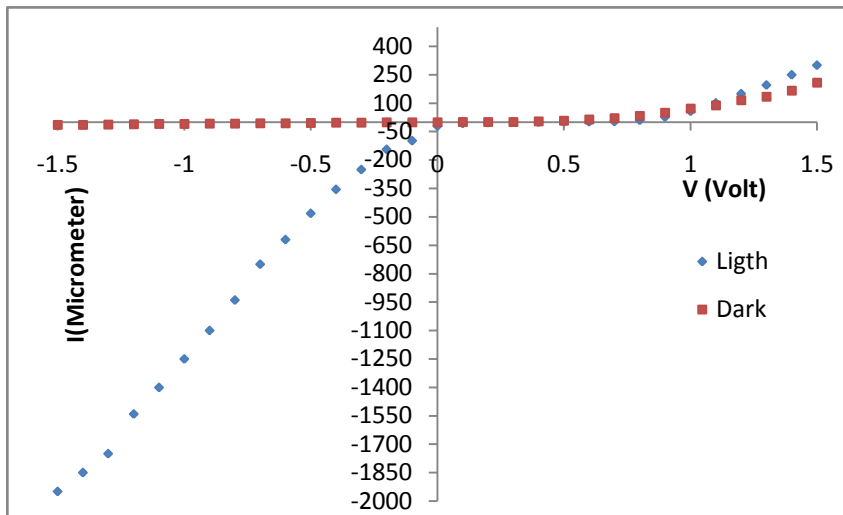


Fig.7 I-V characteristics of Au/Si heterojunction at dark and and light conditions

Also in the dark condition, one can easily distinguish two linear regions in the I-V plot. Under forward bias conditions, the current flows relatively freely in this direction of the diode and the resistance of the photodiode is determined by the series resistance (R_s). The two main components contribute to the resistance, the base layer and the electrical

contacts). In the reverse bias region, really low current flows, the influence of shunt resistance (R_s), which is usually similar to the max value, predominates. The main source of the shunt resistance is a surface leakage current connected with the passivation of the junction (Wenus etel, 2003). In general the forward dark current is generated due to the flow of majority carriers and the applied voltage injects majority carriers, which leads to decrease the value of built in potential, and decrease the width of the depletion layer. The majority and minority carrier concentration is higher than the intrinsic carrier concentration (n_i), i.e $np > n_i^2$ which is leading to generate recombination current at low voltage region (Green, 1989). While the tunneling current is represented in the high voltage region (Migliorato etel, 1982). The mechanism of transport current is estimated from the value of the ideality factor (β), where the value of β equals to one, this indicates minority carrier diffusion, while β equals to two is obtained when generation and recombination of electron-hole pairs in the photodiode depletion region determines the forward dark current (Wenus etel, 2003).

Fig.8 shows the semi-log of the dark forward current as a function of applied voltage (0-0.5) Volt for Si/Au heterojunction. There are two regions can be recognized in this figure. The ideality factor could be calculated from the slope of linear dependence of the first region, while the tunneling constant can be deterred from the slope of the curve in the second region.

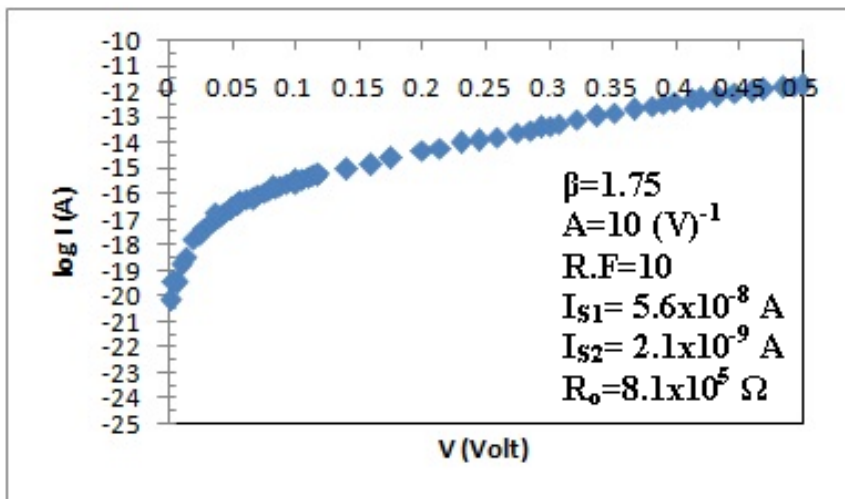


Fig.8 the Au/Si heterojunction parameters that deduced from I-V characteristics in the forward bias voltage

The variation of the photocurrent (IPA) with a bias voltage (V_a) of the Au/Si heterojunction is present in Fig. 9, the measurements are extended out under illumination power density equal to 1000 W/m² at room temperature.

From this figure we observe that the photocurrent increases with increasing the bias voltage. This is happening because increasing the electric field sweeps the carriers out of the depletion region and with existing illumination, electron-hole pairs are created near the junction, the solar cell parameters listed in fig. 9.

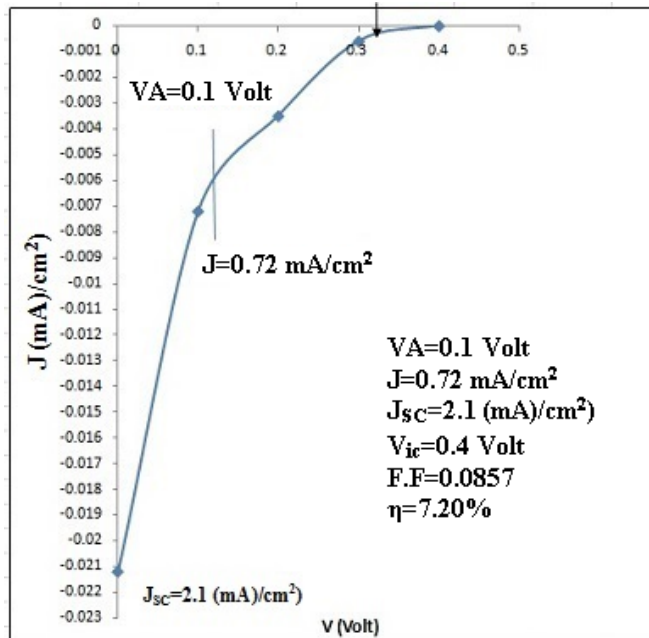


Fig.9 the parameters of Au/Si heterojunction solar cells

CONCLUSIONS

The electrical properties of Au/Si heterojunction solar cells, which included the AC conductivity, C-V and I-V characteristics, have been analyzed. The first one the parameters of heterojunction such as while the second show that, the profile of the heterojunction is abrupt and W , V_D , N , have been calculated as a function of different values of frequency to consider the type of mechanism. Finally the last one show that this heterojunction has rectification properties, the ideality factor was estimated to be 1.75 and the tunneling factor 10 (V)⁻¹, in addition the heterojunction solar cell parameters have been determined such as V_A , I , F.F. The efficiency found to be 7.19%.

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Asian Journal of Applied Science and Engineering

(Multidisciplinary peer reviewed international journal)

ISSN: 2305-915X (print); 2307-9584 (Online)
ICV 5.20; SJIF 2.607; UIF 2.0476

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